REMARKS

Claims 2 and 3 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **April 4, 2003**.

Claims 1-3 and 5-9 remain in this application. Claims 1, 5 and 9 have been allowed, claim 4 has been cancelled, and claims 6-8 have been withdrawn.

Claim Rejections under 35 USC §103

Claims 2 and 3 are rejected under 35 USC §103(a) as being unpatentable over Bryant et al. (U.S. Patent No. 6,100,564) in view of Shirai (U.S. Patent No. 5,422,505).

First, referring to Bryant et al., as stated in item 3 of the Office Action, Bryant et al. discloses, especially in Fig. 4C and Fig. 5, "an insulated gate type semiconductor device comprised of a semiconductor layer 103 serving as an active region isolated from a semiconductor substrate 101 by a substrate isolation insulating film 102, wherein an insulating film 109 is provided on a surface of a first conductivity type semiconductor region positioned at an interface between that first conductivity type body contact region 113 and a second conductivity type source 211 and drain 212 regions and directly under a gate electrode 112, said gate electrode being provided on the region except for said body contact region."

However, as understood from item 3 of the Office Action, Bryant et al. does not disclose that an insulating film provided on the surface of a first conductivity type semiconductor

region positioned at an interface between a first conductivity type body contact region and a second conductivity type source and drain regions is made greater than the thickness of a gate insulating film directly under a gate electrode.

That is, the Examiner insists, in item 3 of the Office Action, that "Shirai discloses, in Fig. 3, an insulating film 14' provided on a surface of a first conductivity type semiconductor region positioned at an interface between a first conductivity type body contact region 13'-4, 13-4 and a second conductivity type source 16' and drain 16 regions is made greater than the thickness of a gate insulating film directly under a gate electrode."

However, the regions 13'-4 and 13-4 shown in Fig. 3 of Shirai are both channel regions and positioned under the gate electrode G' through the gate insulating film 14, (a) the above region 13-4 is a channel region at one source/drain region 16 and (b) the above region 13'-4 is a channel region at the other source/drain region 16'.

Accordingly, these regions 13'-4 and 13-4 are not a body contact region as described in item 3 of the Office Action, but a channel region. Please note that, in general, the body contact region is located at a region other than a channel region.

Further, since the filed effect transistor disclosed in Shirai is not an insulated gate type semiconductor device (SOI type semiconductor device) to which the present invention is applied, it is originally unnecessary to provide such a body contact region as shown in the present invention.

Thus, Shirai does not disclose that "the thickness of an insulating film, particularly the thickness of an insulating film provided on the surface of a first conductivity type semiconductor region positioned at an interface between a first conductivity type body contact region positioned

at a region other than a region forming a gate electrode and a second conductivity type source and drain regions, is made greater than the thickness of a gate insulating film directly under the gate electrode", as defined in claims 2 and 3 of the present application.

Accordingly, the Examiner assertion that the inventions of the current claims 2 and 3 of the present application would be unpatentable over Bryant et al. and Shirai is respectfully traversed.

Further, in the outstanding Office Action, the Office has specifically stated that "Shirai discloses in Fig. 3, an insulating film 14' provided on a surface of a first conductivity type semiconductor region." In column 5 line 3, reference numeral 14' is disclosed to be a gate insulating film.

It should be noted that, as clearly depicted in Figure 3 of Shirai, what the Office regards to be the gate insulating film 14' has a varying thickness. In contradistinction, as clearly shown in Figure 1(b) of the present invention, the gate insulating film 4 has a uniform thickness.

To further patentably distinguish over the asserted prior art references, claims 2-3 have been further amended to recite that "a gate insulating film with a uniform thickness." By so amending, claims 2-3 are placed in condition for allowance.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number

indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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